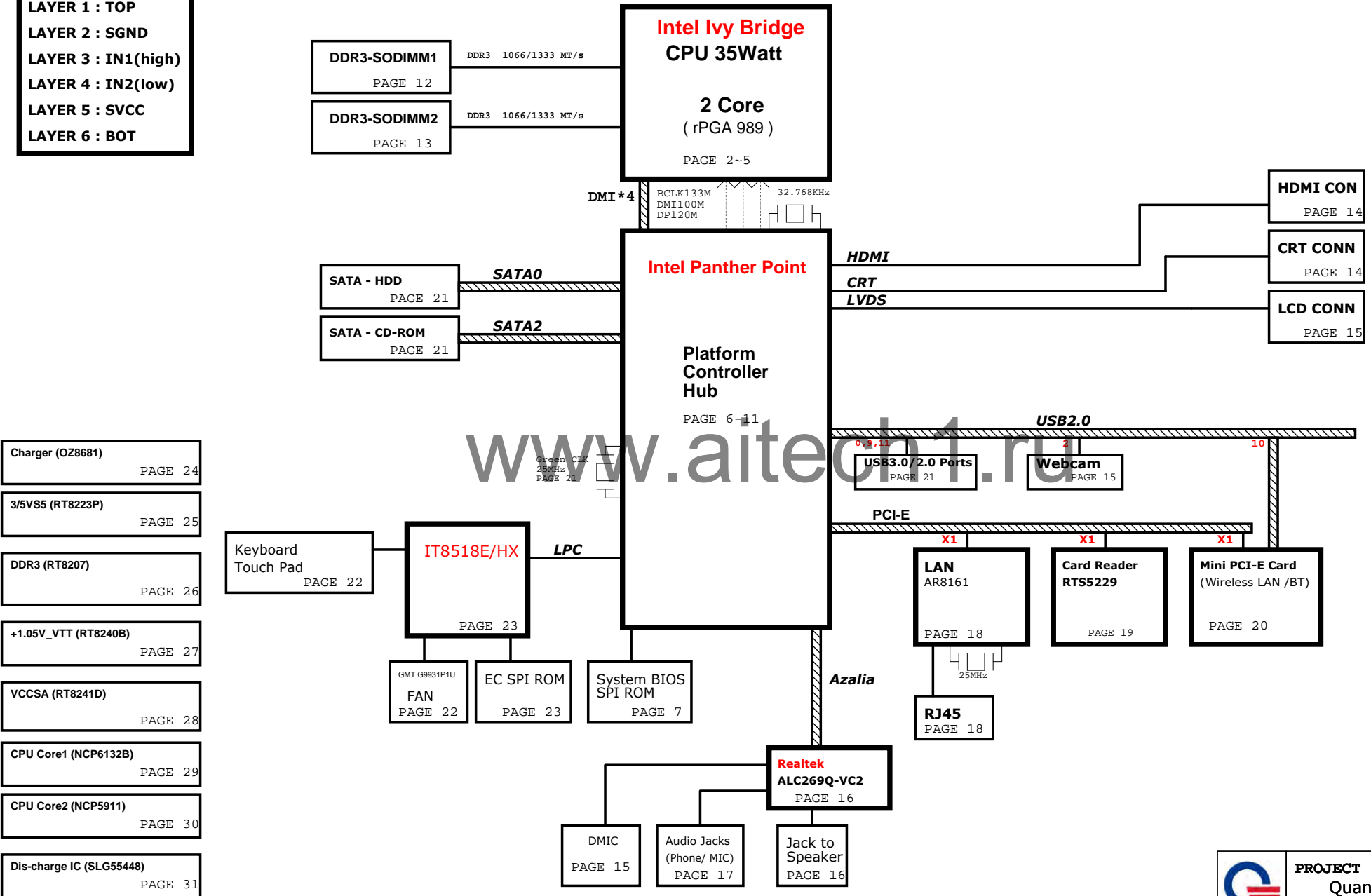


SW6C UMA (14") BLOCK DIAGRAM

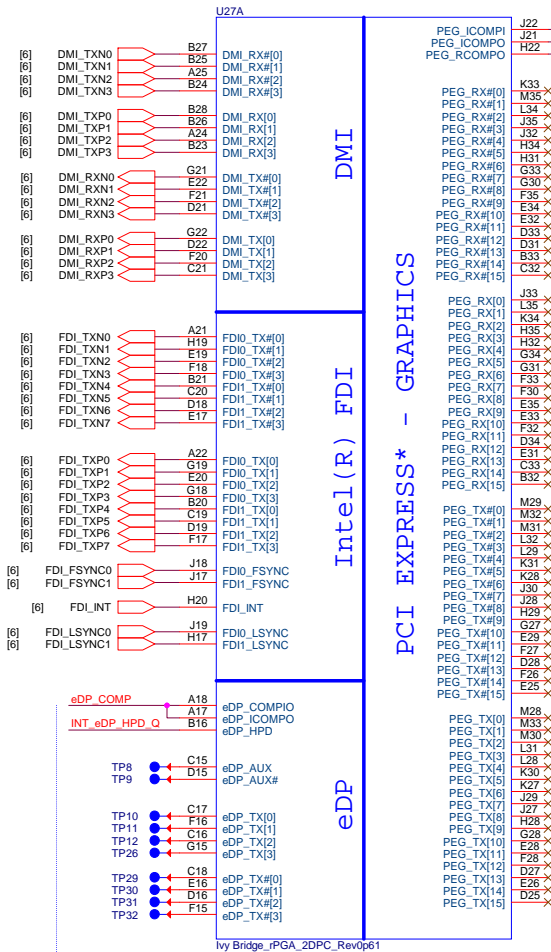
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(high)
- LAYER 4 : IN2(low)
- LAYER 5 : SVCC
- LAYER 6 : BOT



Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)



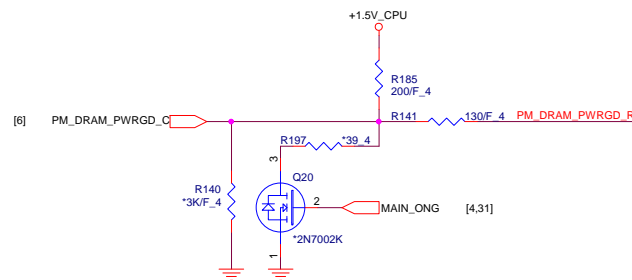
eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
 eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

+1.05V_VTT R481 24.9/F 4 eDP_COMP
 +1.05V_VTT R81 24.9/F 4 PEG_COMP

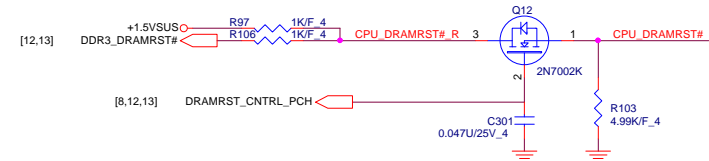
eDP_HPD can be left as no connect if entire eDP is disabled.

+1.05V_VTT R482 10K/F 4 INT_eDP_HPD_Q

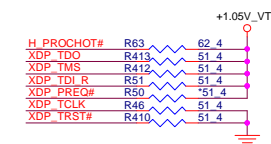
SM_DRAMPWROK Processor Input.



DDR3 DRAM RESET

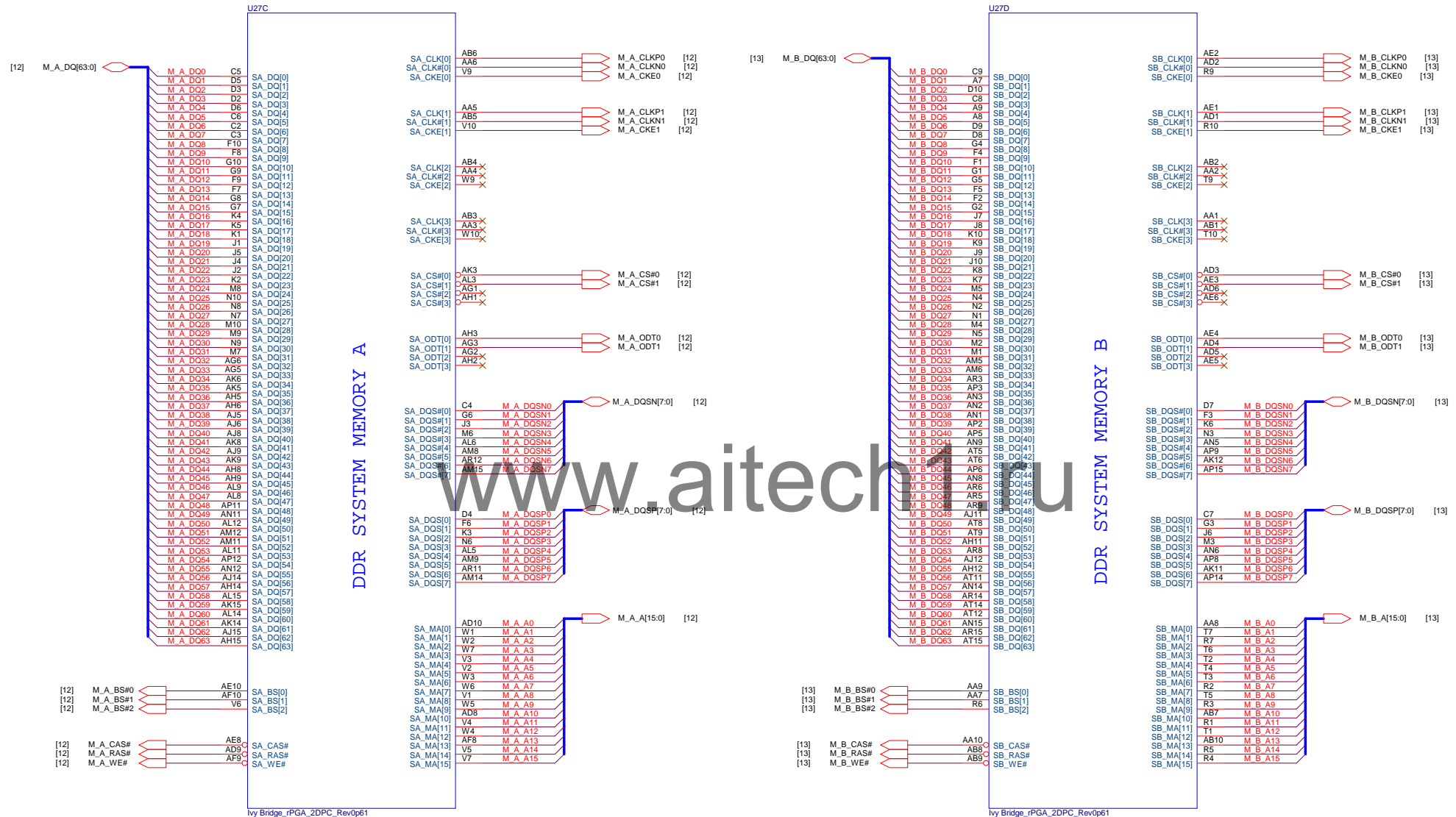


Processor pull-up (CPU)

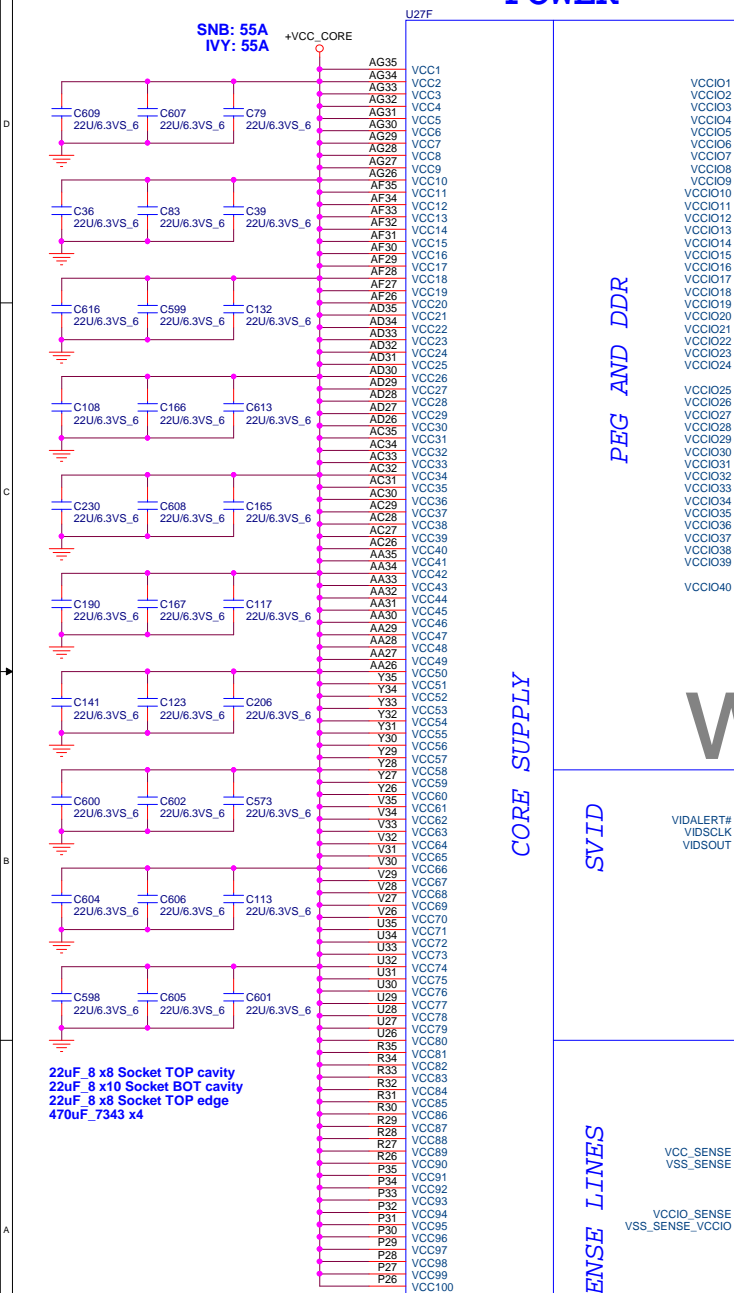


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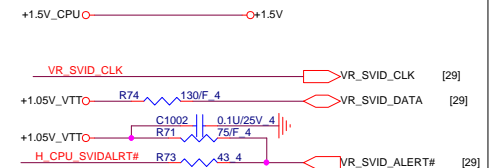
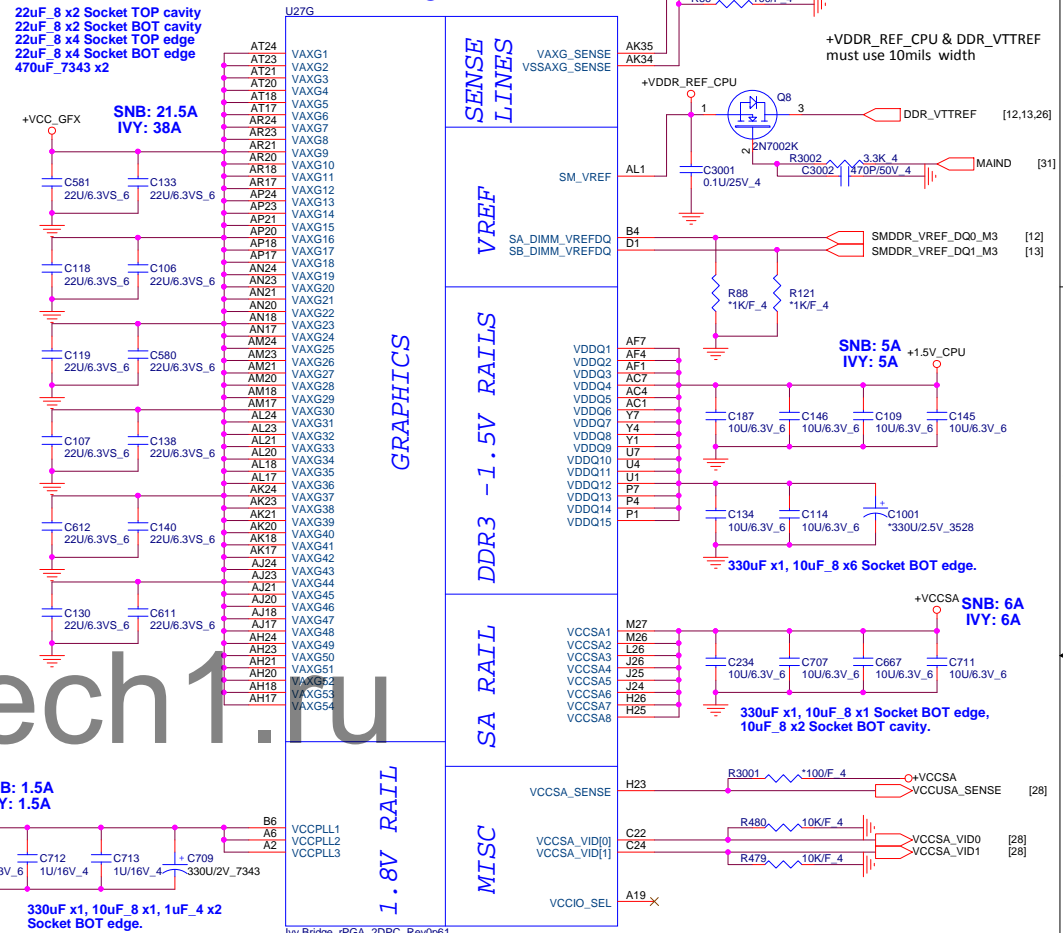
Ivy Bridge Processor (DDR3)



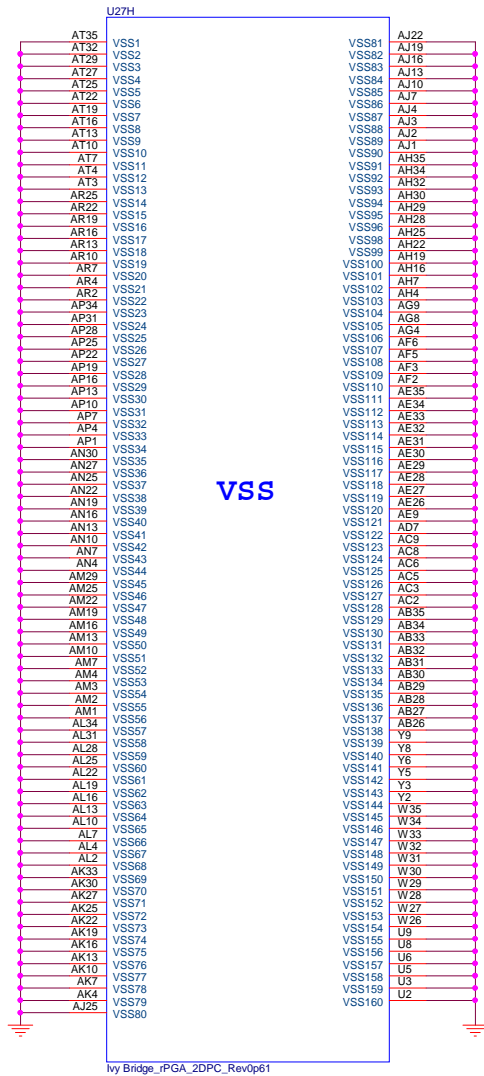
POWER



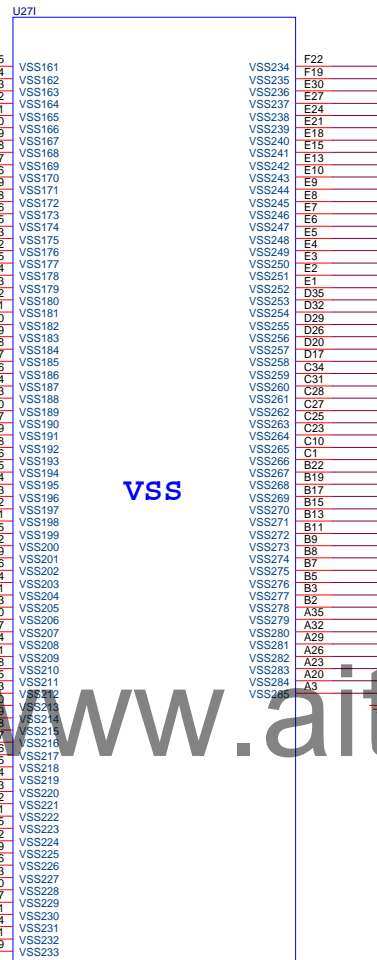
POWER



Ivy Bridge Processor (GND)

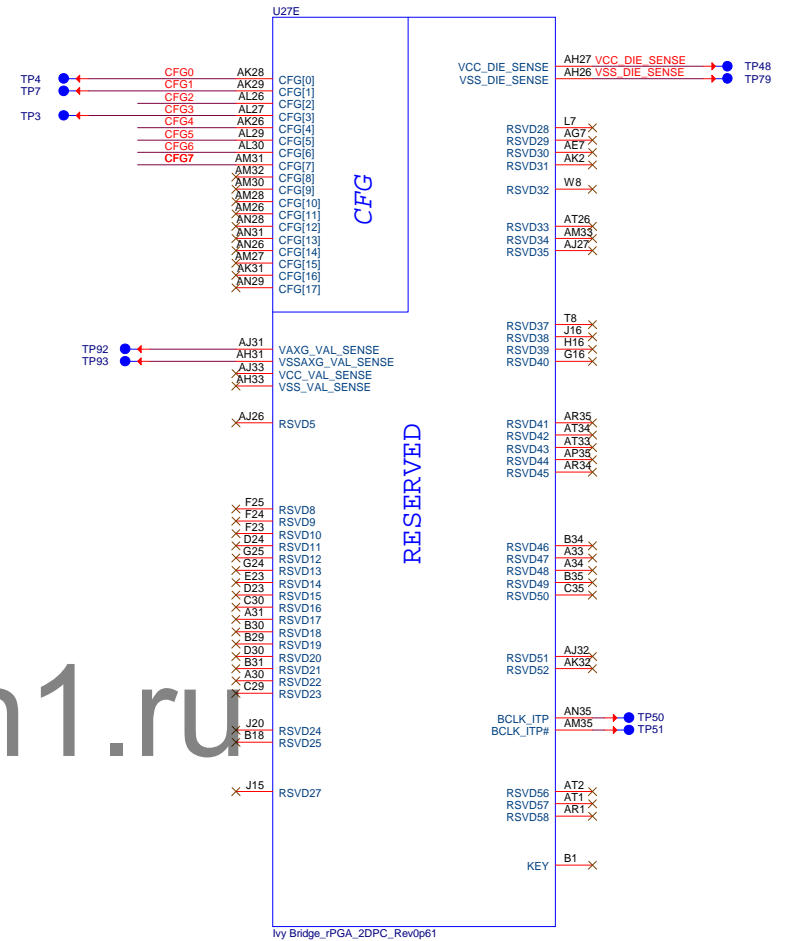


Ivy Bridge_rPGA_2DPC_Rev0p61



Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge Processor (RESERVED, CFG)



Ivy Bridge_rPGA_2DPC_Rev0p61

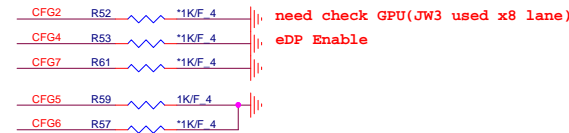
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

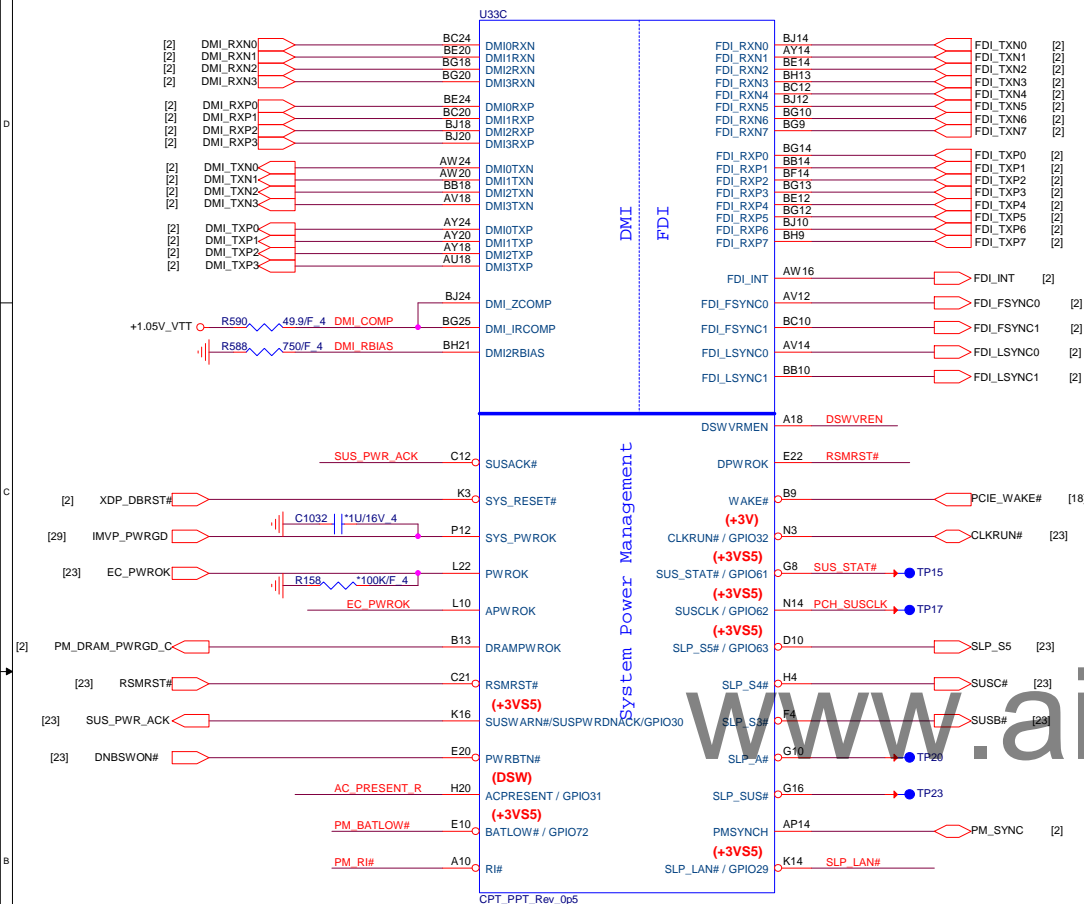
| | 1 | 0 |
|---|---|--|
| CFG2 (PCIe Static x16 Lane Numbering Reversal) | Normal Operation(Default) | Lane Reversed |
| CFG4 (DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |



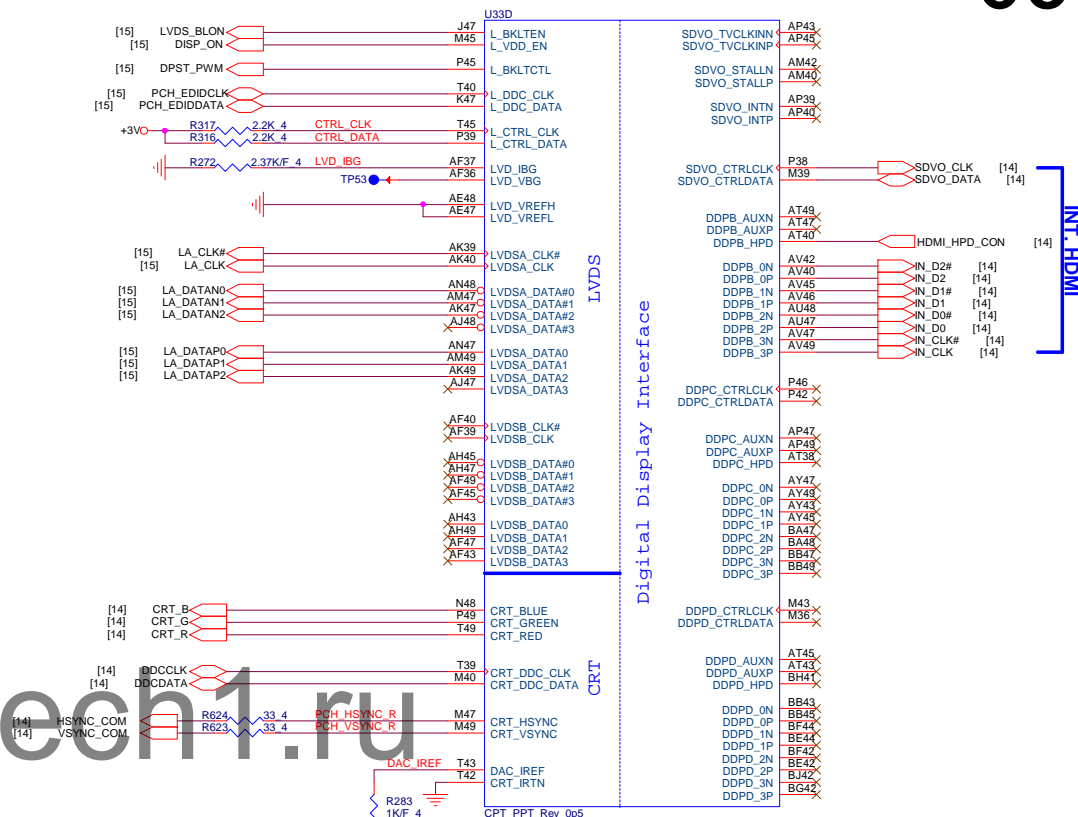
PROJECT : SW6C
Quanta Computer Inc.

| | | |
|--|---|-----------|
| Size | Document Number SNB 4/4 (GND) | Rev 1A |
| Date: Tuesday, November 20, 2012 Sheet 5 of 34 | | |

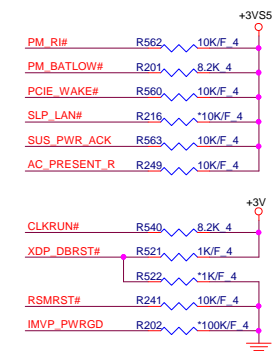
Panther Point (DMI, FDI, PM)



Panther Point (LVDS, DDI, CRT)

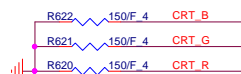


PCH Pull-high/low(CLG)



PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.



System PWR_OK(CLG)

+3V_RTC R583 330K/F_4 DSWVREN

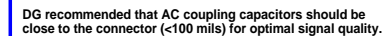
| |
|--|
| On Die DSW VR Enable |
| High = Enable (Default) Low = Disable |



PROJECT : SW6C
Quanta Computer Inc.

| | | |
|----------------------------------|--|-----------|
| Size | Document Number PCH 1/6 (DM/FDI/VIDEO) | Rev 1A |
| Date: Tuesday, November 20, 2012 | Sheet 6 of 34 | |

07



30mils

+3V_RTC

RTC_RS

SRTC_RS

R357
20K/F_4

R362
20K/F_4

R358
20K/F_4

C503
1U/16V_4

C506
1U/16V_4

C517
1U/16V_4

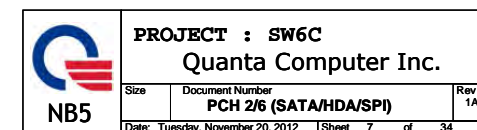
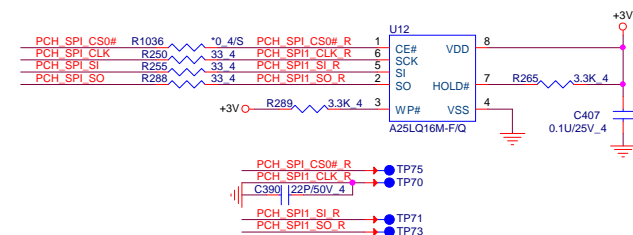
RTC_RS#

SRTC_RS#

RTC Power trace width 20mils.

| Pin Name | Strap description | Sampled | Configuration | Circuit | | | | | | | | | |
|---------------------|--|---------------|--|--------------|-------|---------------|---|---|-----|--|--|-----|--|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode | | | | | | | | | | |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode 1 = Default (weak pull-up 20K) | | | | | | | | | | |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | | | | | | | | | | |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security Only for Interposer | PWROK | 0 = Override 1 = Default (weak pull-up 20K) | | | | | | | | | | |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | <table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>SPI</td></tr> <tr> <td></td><td></td><td>LPC</td></tr> </tbody> </table> | GNT1# | GNT0# | Boot Location | 0 | 0 | SPI | | | LPC | (Need external pull-down for LPC BIOS) |
| GNT1# | GNT0# | Boot Location | | | | | | | | | | | |
| 0 | 0 | SPI | | | | | | | | | | | |
| | | LPC | | | | | | | | | | | |
| GPIO19 | Boot BIOS Selection 0 [bit-0] | PWROK | Default weak pull-up on GNT0/1# | | | | | | | | | | |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 20K) | USE GPIO PIN | | | | | | | | | |
| NV_ALE | Intel Anti-Theft HDD protection Only for Interposer | PWROK | 0 = Disable (Internal pull-down 20kohm) | | | | | | | | | | |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 20kohm | | | | | | | | | | |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V | | | | | | | | | | |
| HDA_SDO | Flash Descriptor Security | PWROK | 0 = Override 1 = Default (weak pull-up 20K) | | | | | | | | | | |
| GPIO8 | Integrated Clock Chip Enable | RSMRST# | Should be pull-down (weak pull-up 20K) | | | | | | | | | | |
| GPIO28 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable 1 = Enable (Default) | | | | | | | | | | |
| SPI_MOSI | iTPM function Disable | APWROK | 0 = Default (weak pull-down 20K) 1 = Enable | | | | | | | | | | |

PCH SPI ROM(CLG)

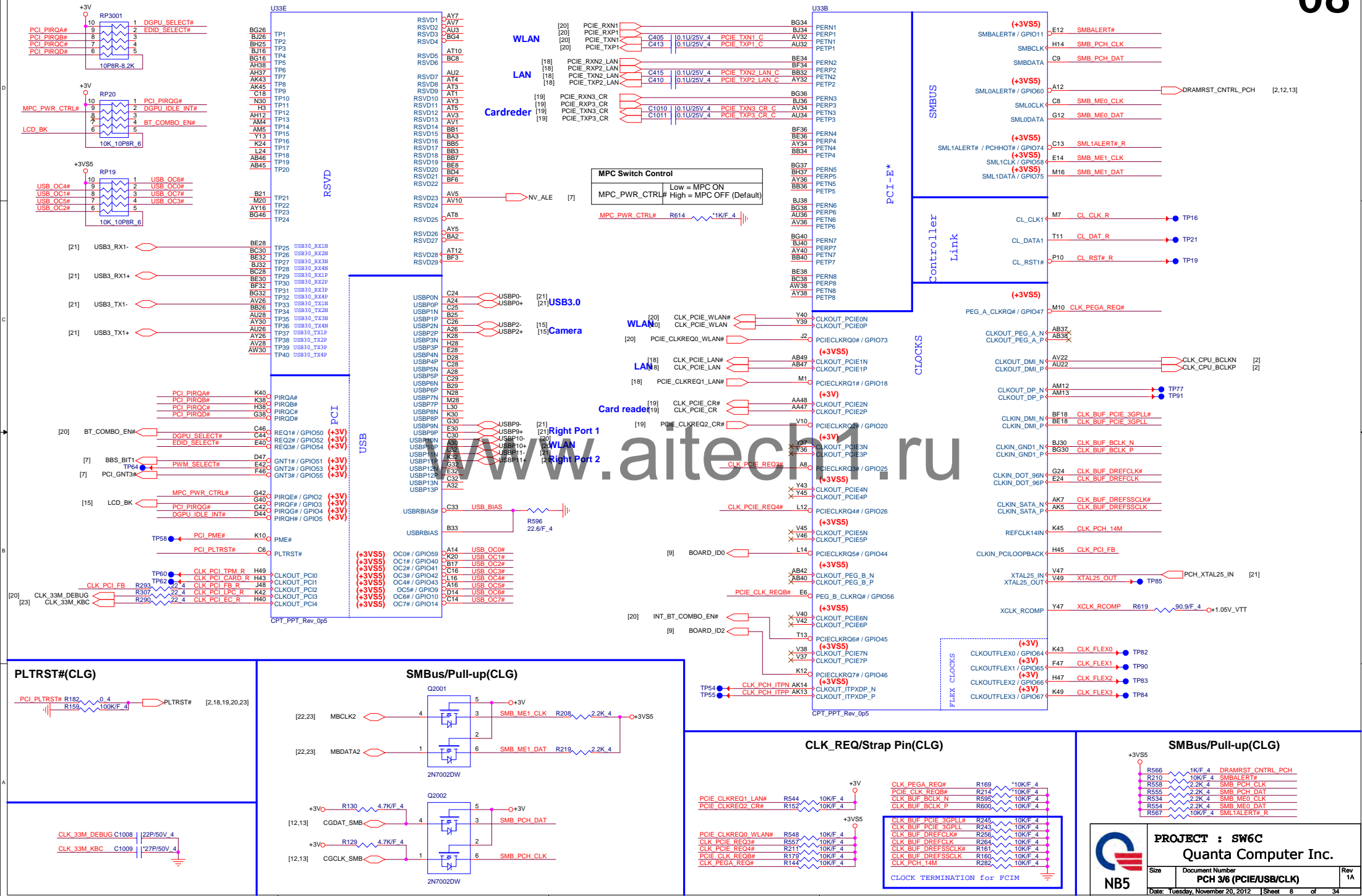


PCI/USBOC# Pull-up(CLG)

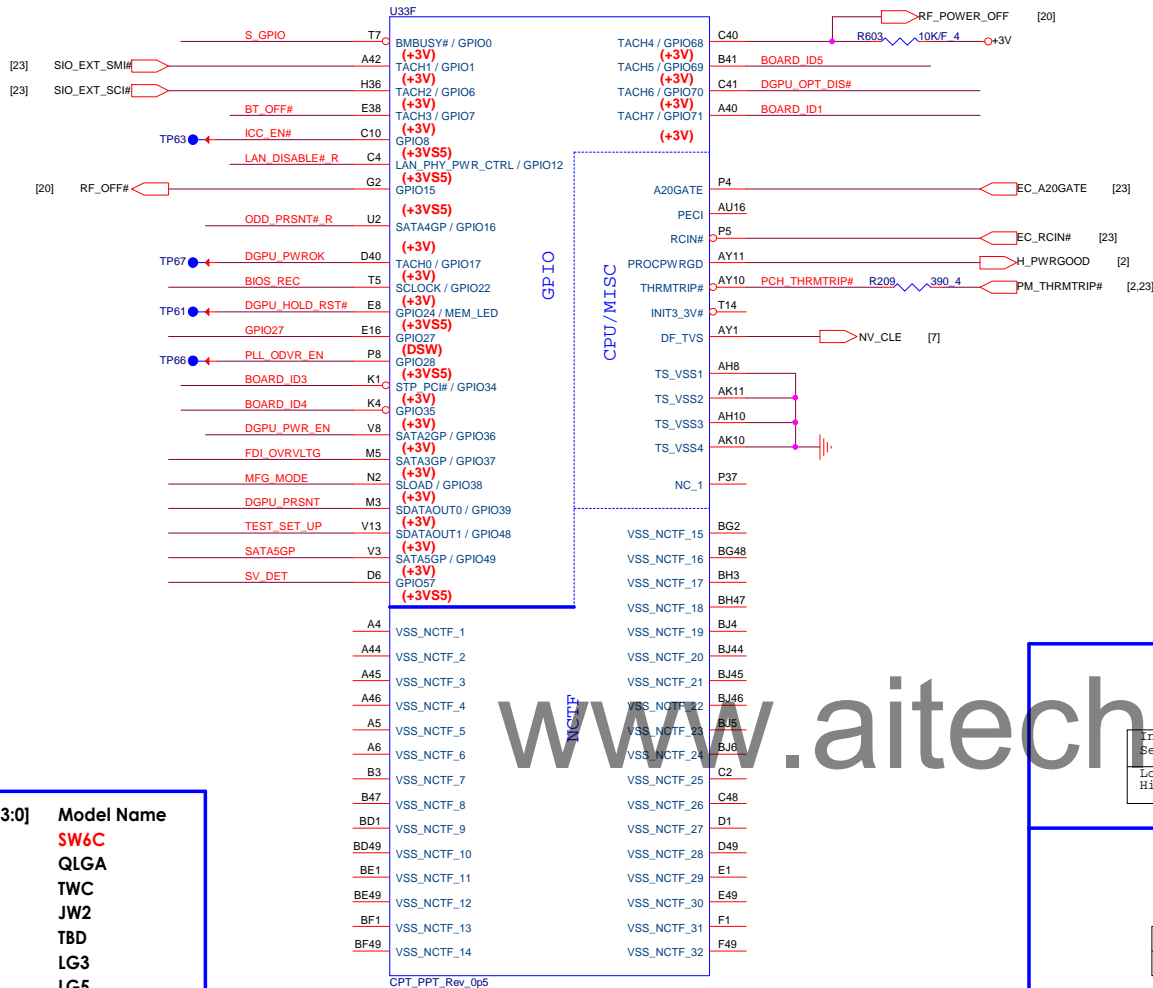
Panther Point (PCI,USB)

Panther Point (PCI-E, SMBUS, CLK, CL)

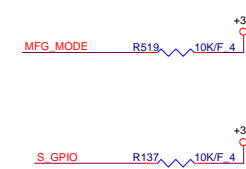
08



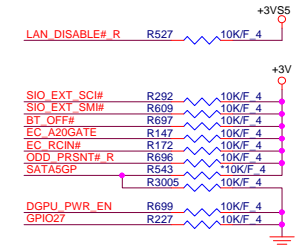
Panther Point(GPIO,VSS_NCTF,MISC)



MFG-TEST



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

BIOS RECOVERY High = Disable (Default)

Low = Enable

TEST SET UP High = Strong (Default)

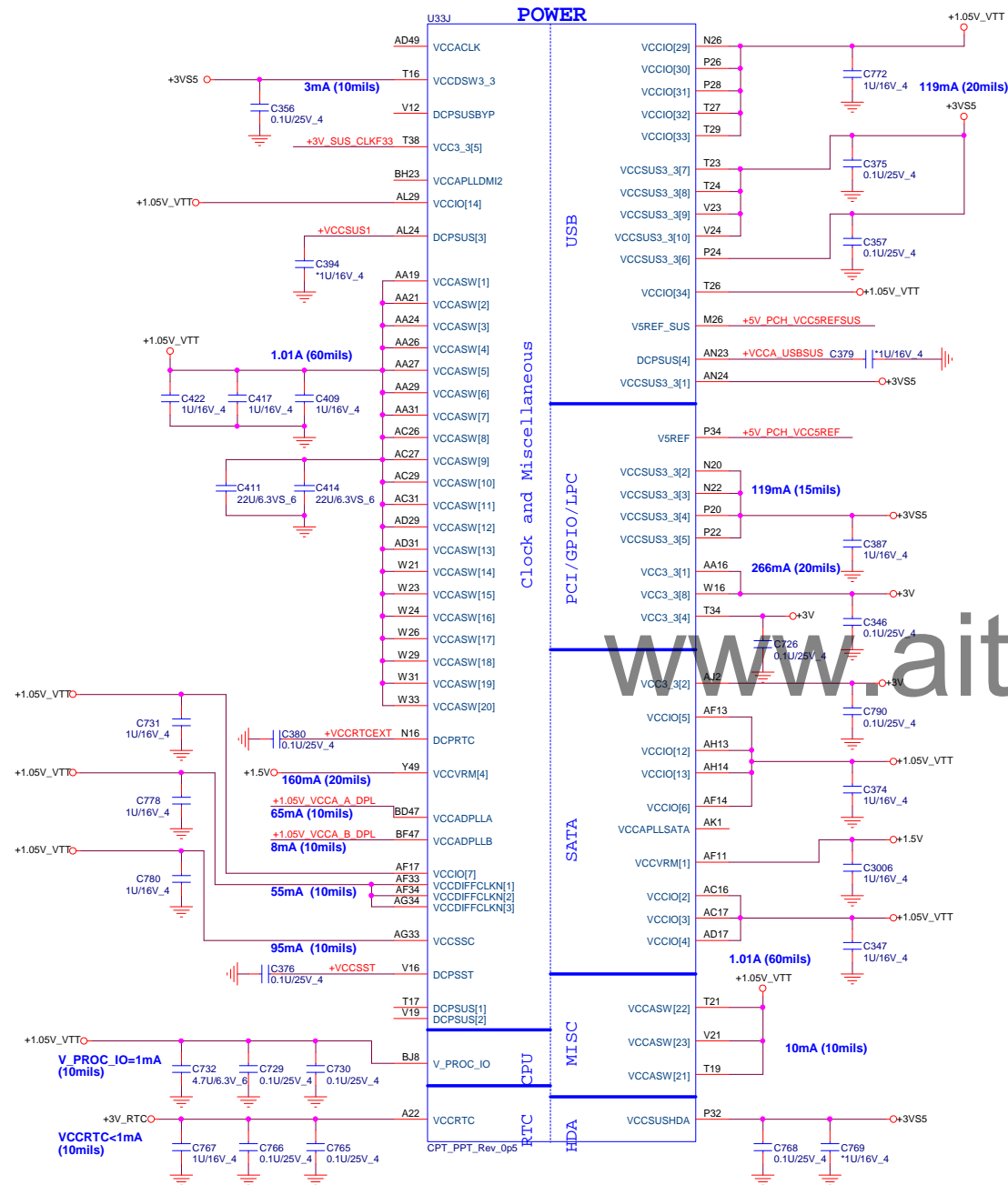
TEST DETECT Low = Default

20110926 Reserved only

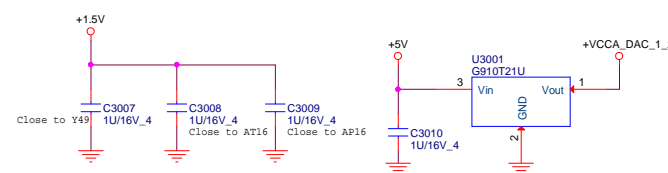
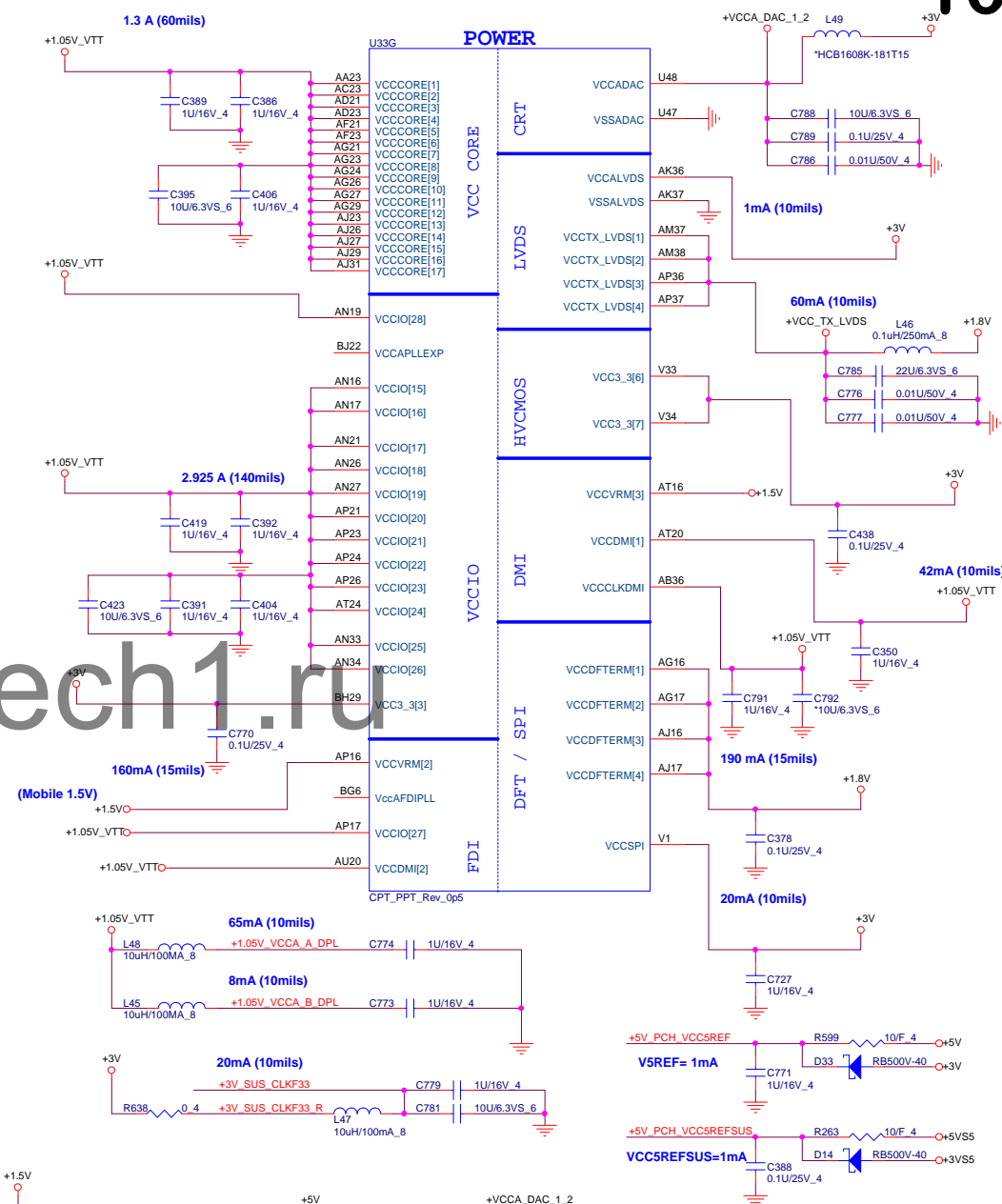
FDI_OVRVLTG LOW - Tx, Rx terminated to same voltage

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Panther Point (POWER)

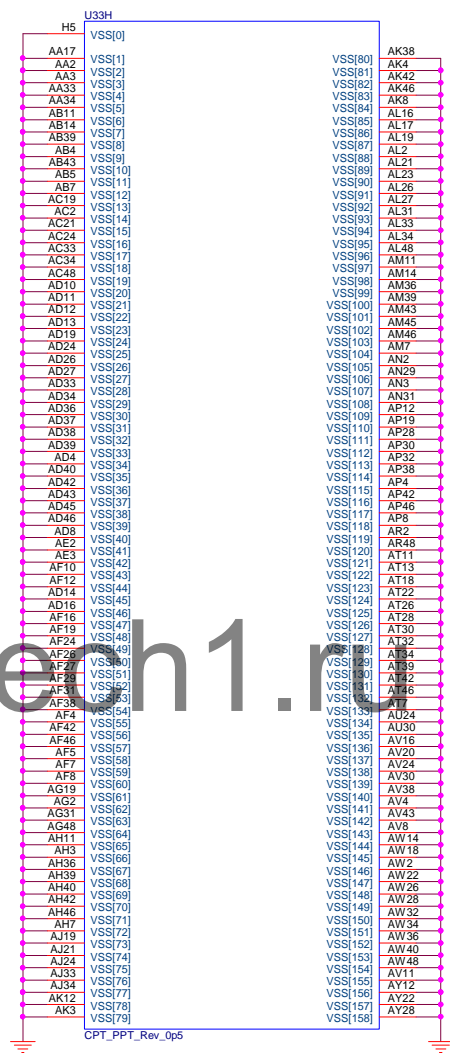
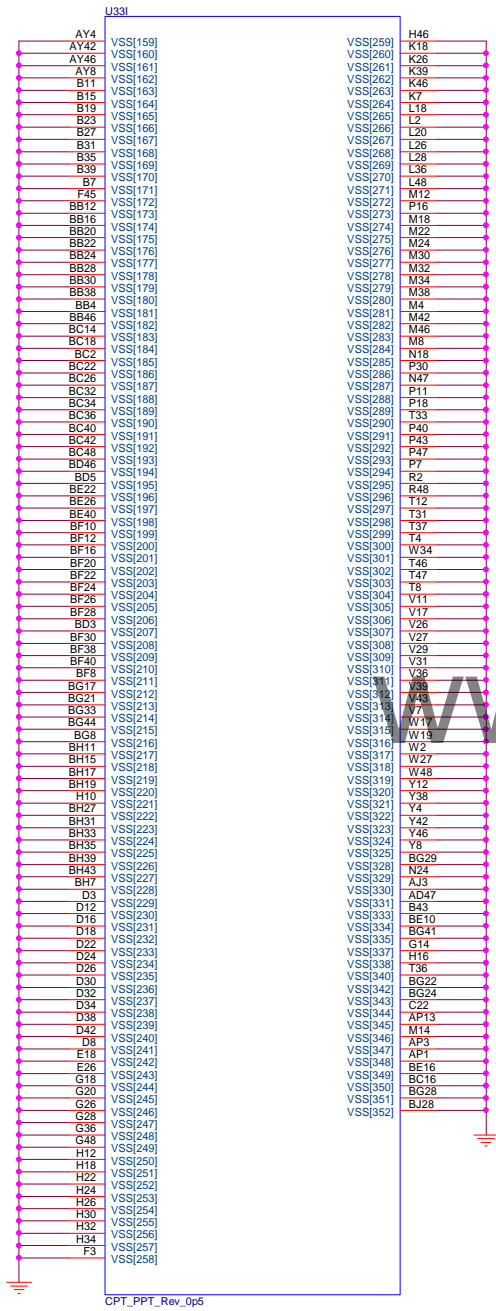


Panther Point (POWER)



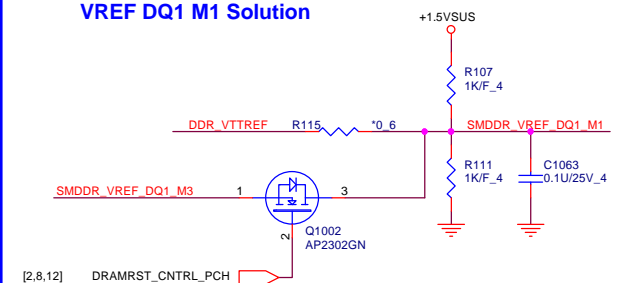
Panther Point (GND)

Panther Point (GND)

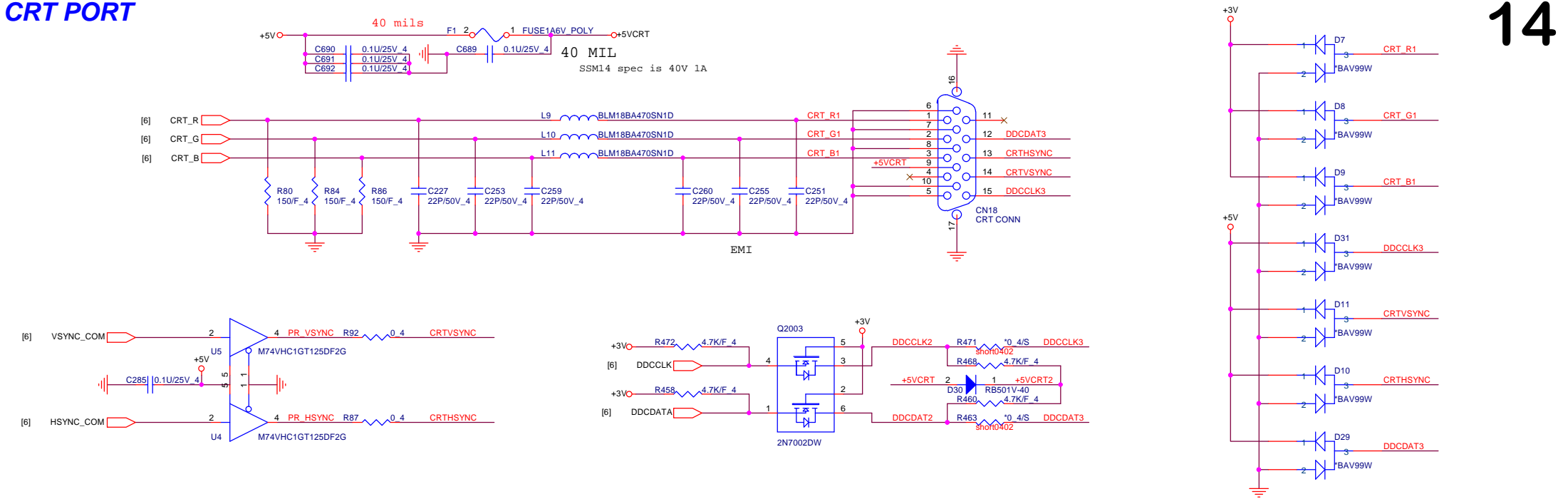




VREF DQ1 M1 Solution

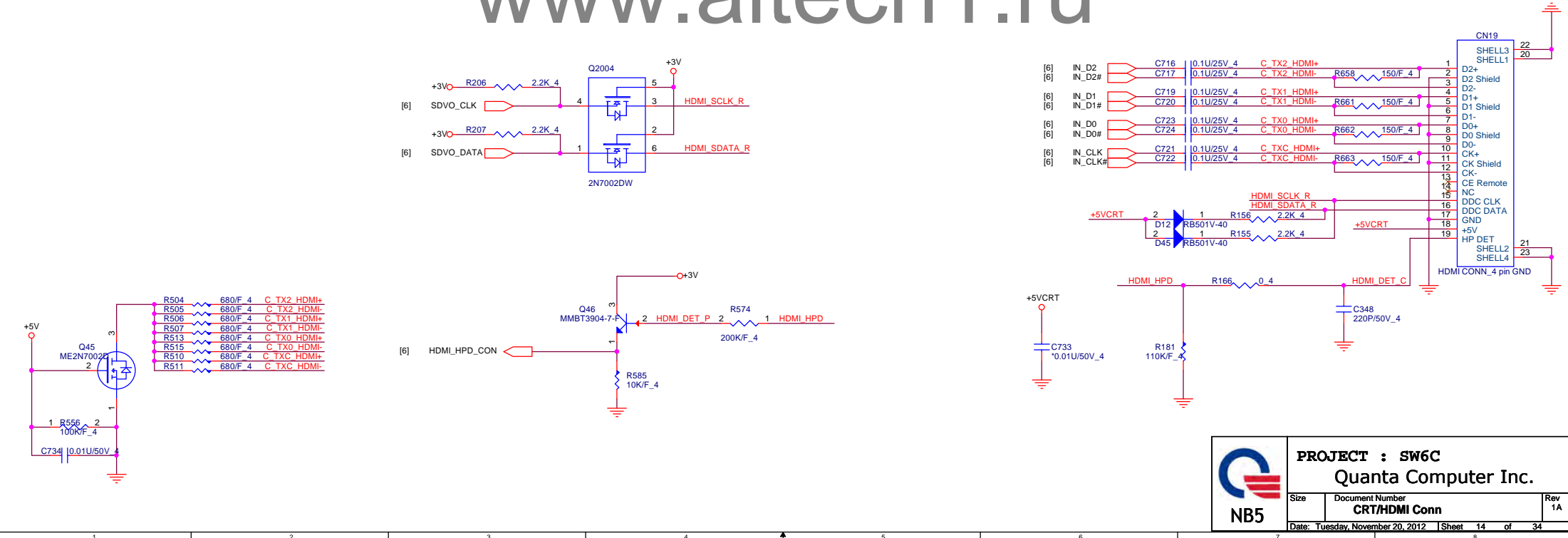


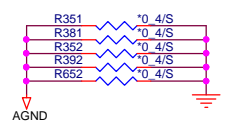
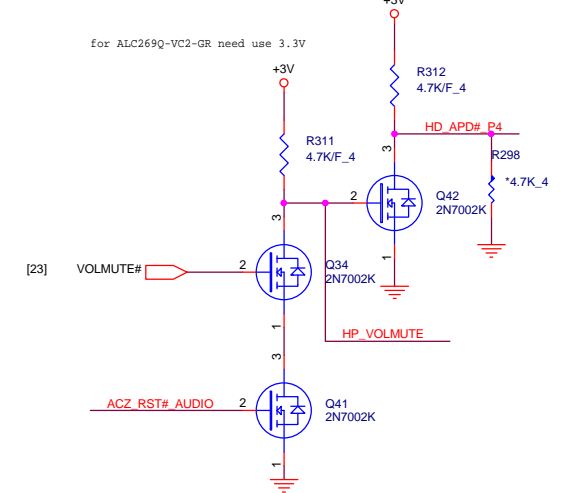
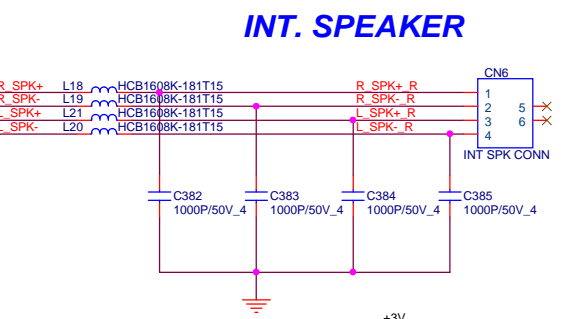
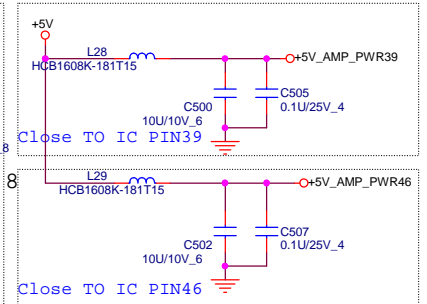
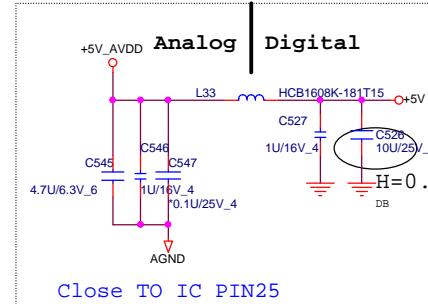
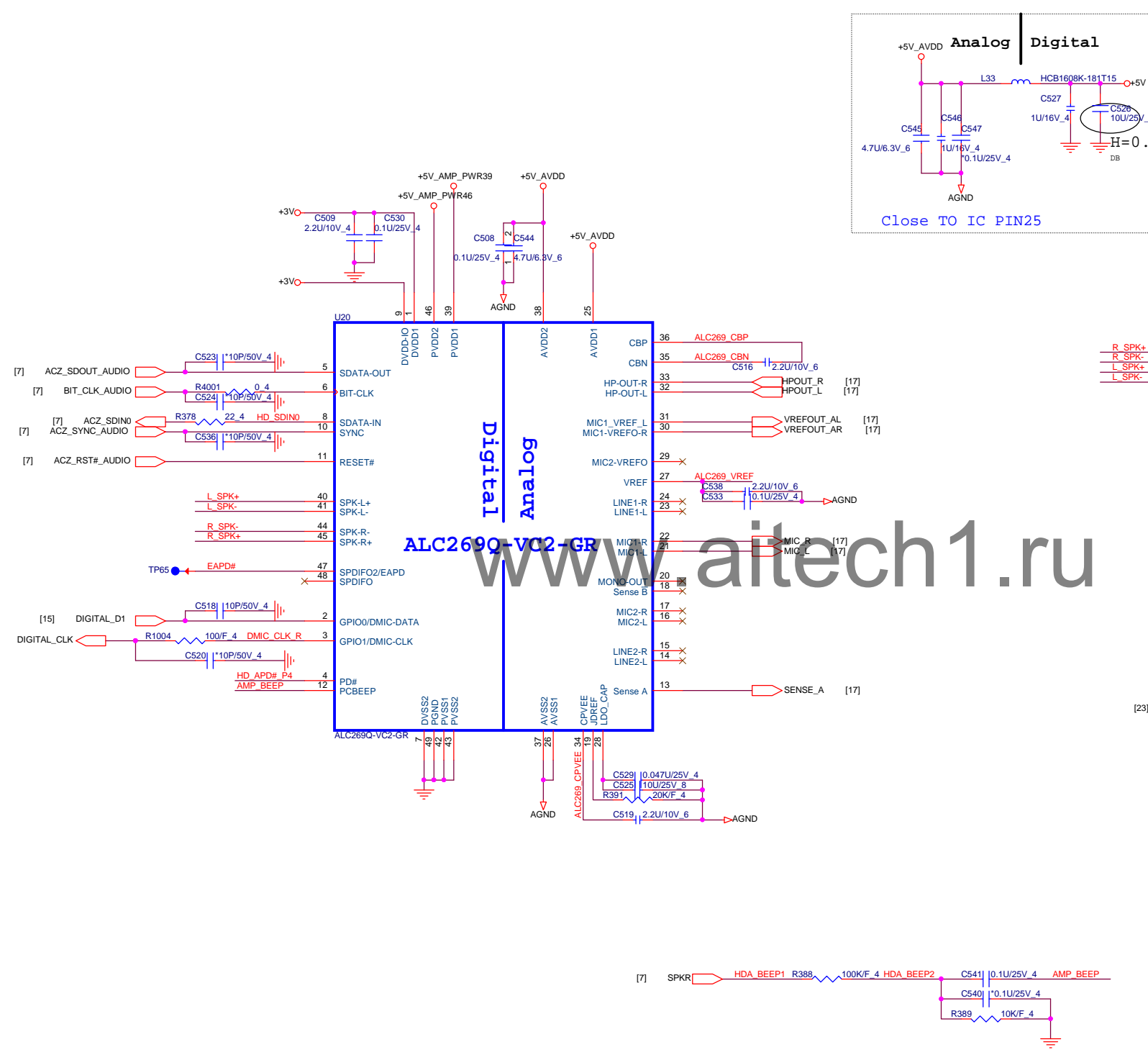
CRT PORT

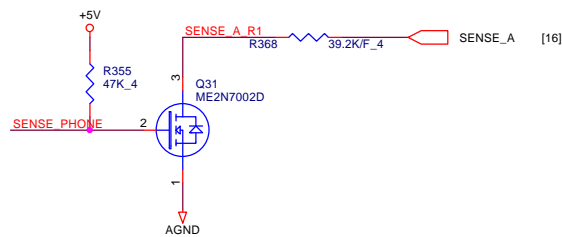


HDMI PORT

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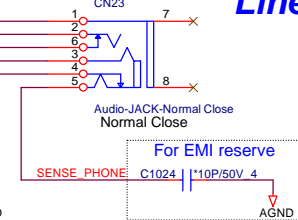
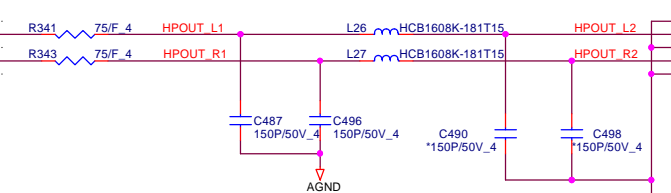




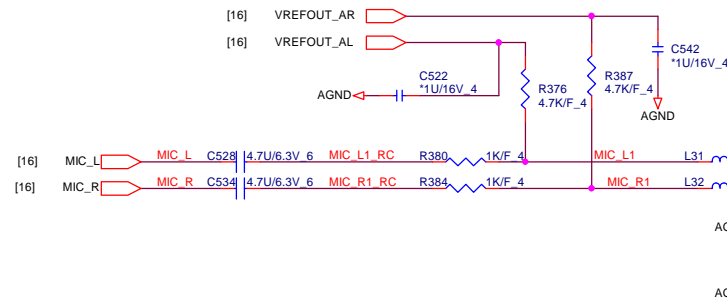
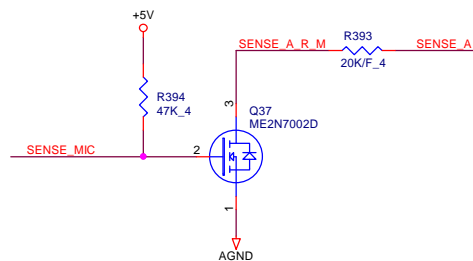


AGND SHIELD
AGND SHIELD
AGND SHIELD

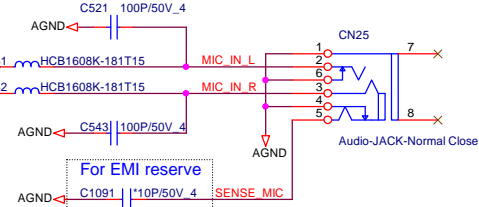
[16] HPOUT_L
[16] HPOUT_R



Line out 17

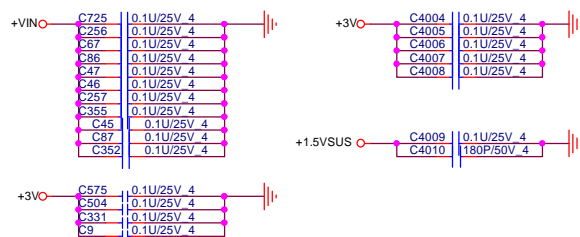


MIC

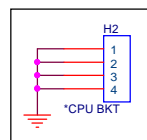


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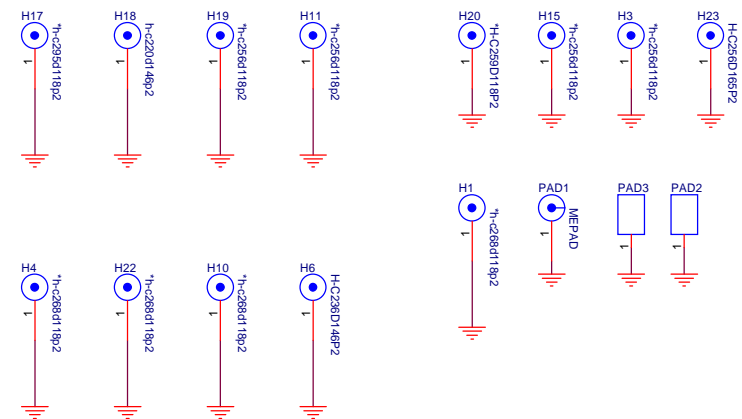
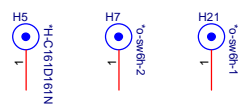
EMI



CPU



NPTH

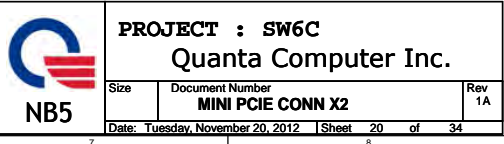


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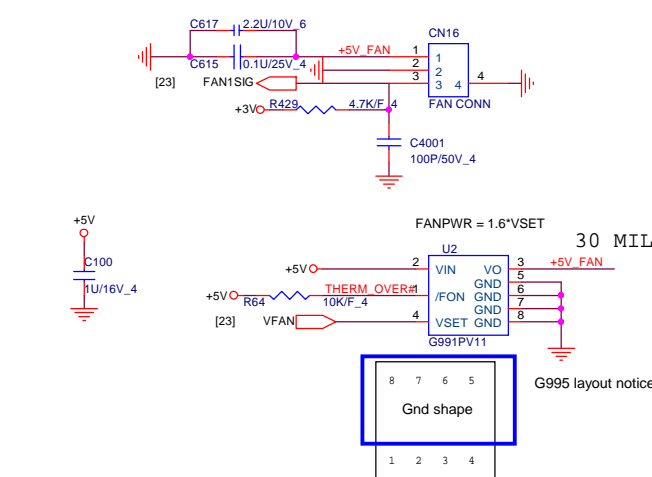
The diagram shows the CM3R-065 module with the following connections:

- Pin 11:** +3V3CARD
- Pin 22:** +3V3CARD
- Pin 4:** 5V (connected to 5V regulator)
- Pin 23:** 5V (connected to 5V regulator)
- Pin 1:** SD D0
- Pin 2:** SD D1
- Pin 3:** SD D2
- Pin 4:** SD D3
- Pin 5:** SD CLK
- Pin 6:** SD CMD
- Pin 7:** SD CD#
- Pin 8:** SD WP
- Pin 9:** GND
- Pin 10:** GND
- Pin 12:** MS D0
- Pin 13:** MS D1
- Pin 14:** MS D2
- Pin 15:** MS D3
- Pin 16:** MS CLK
- Pin 17:** MS IN#
- Pin 18:** MS BS
- Pin 19:** MS-VCC
- Pin 20:** MS-DATA0
- Pin 21:** MS-DATA1
- Pin 22:** MS-DATA2
- Pin 23:** MS-DATA3
- Pin 24:** MS-SCLK
- Pin 25:** MS-INS
- Pin 26:** MS-BS
- Pin 27:** SD-VCC
- Pin 28:** SD-DATA0
- Pin 29:** SD-DATA1
- Pin 30:** SD-DATA2
- Pin 31:** SD-DATA3
- Pin 32:** SD-CLK
- Pin 33:** SD-CMD
- Pin 34:** SD-CD-SW
- Pin 35:** SD-WP-SW
- Pin 36:** GND
- Pin 37:** GND
- Pin 38:** GND
- Pin 39:** GND
- Pin 40:** GND
- Pin 41:** GND
- Pin 42:** GND
- Pin 43:** GND
- Pin 44:** GND
- Pin 45:** GND
- Pin 46:** GND
- Pin 47:** GND
- Pin 48:** GND
- Pin 49:** GND
- Pin 50:** GND
- Pin 51:** GND
- Pin 52:** GND
- Pin 53:** GND
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- Pin 55:** GND
- Pin 56:** GND
- Pin 57:** GND
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- Pin 91:** GND
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- Pin 93:** GND
- Pin 94:** GND
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- Pin 108:** GND
- Pin 109:** GND
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- Pin 111:** GND
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- Pin 151:** GND
- Pin 152:** GND
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- Pin 210:** GND
- Pin 211:** GND
- Pin 212:** GND
- Pin 213:** GND
- Pin 214**

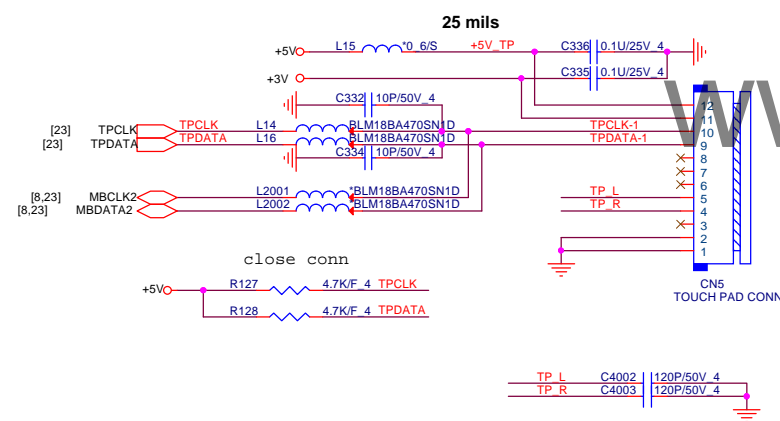




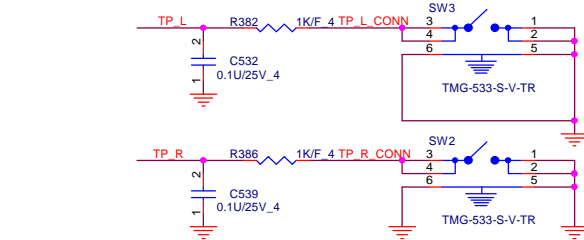
CPU FAN



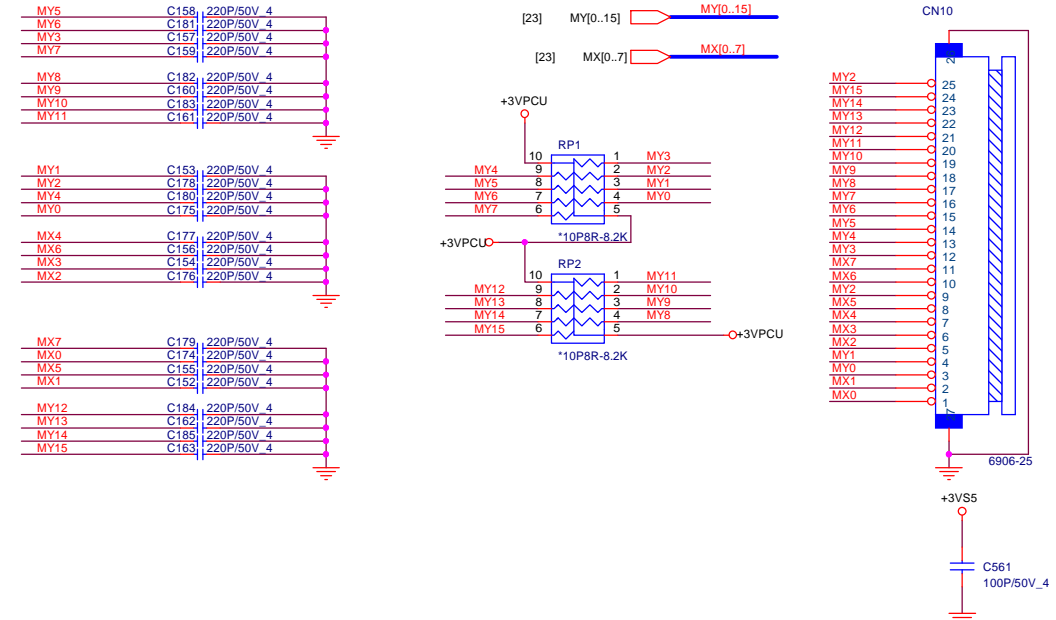
TOUCH PAD



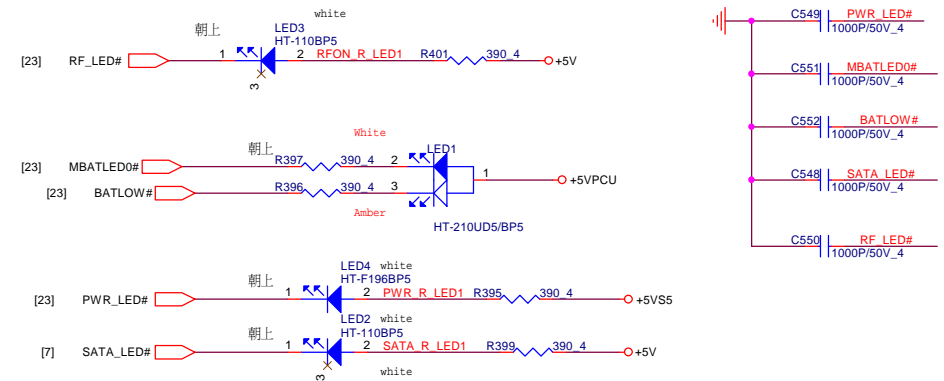
TOUCH PAD L/R

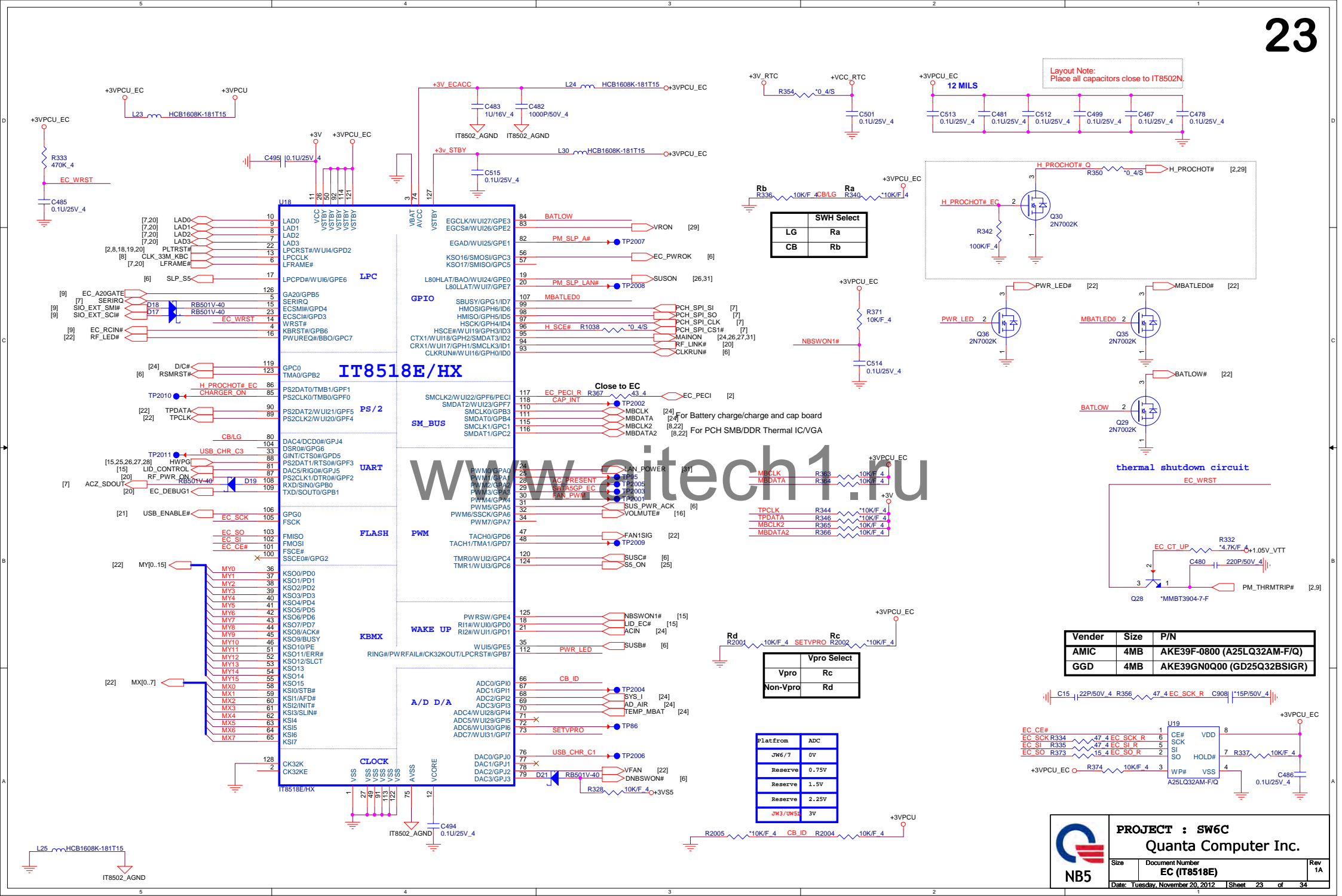


KEYBOARD

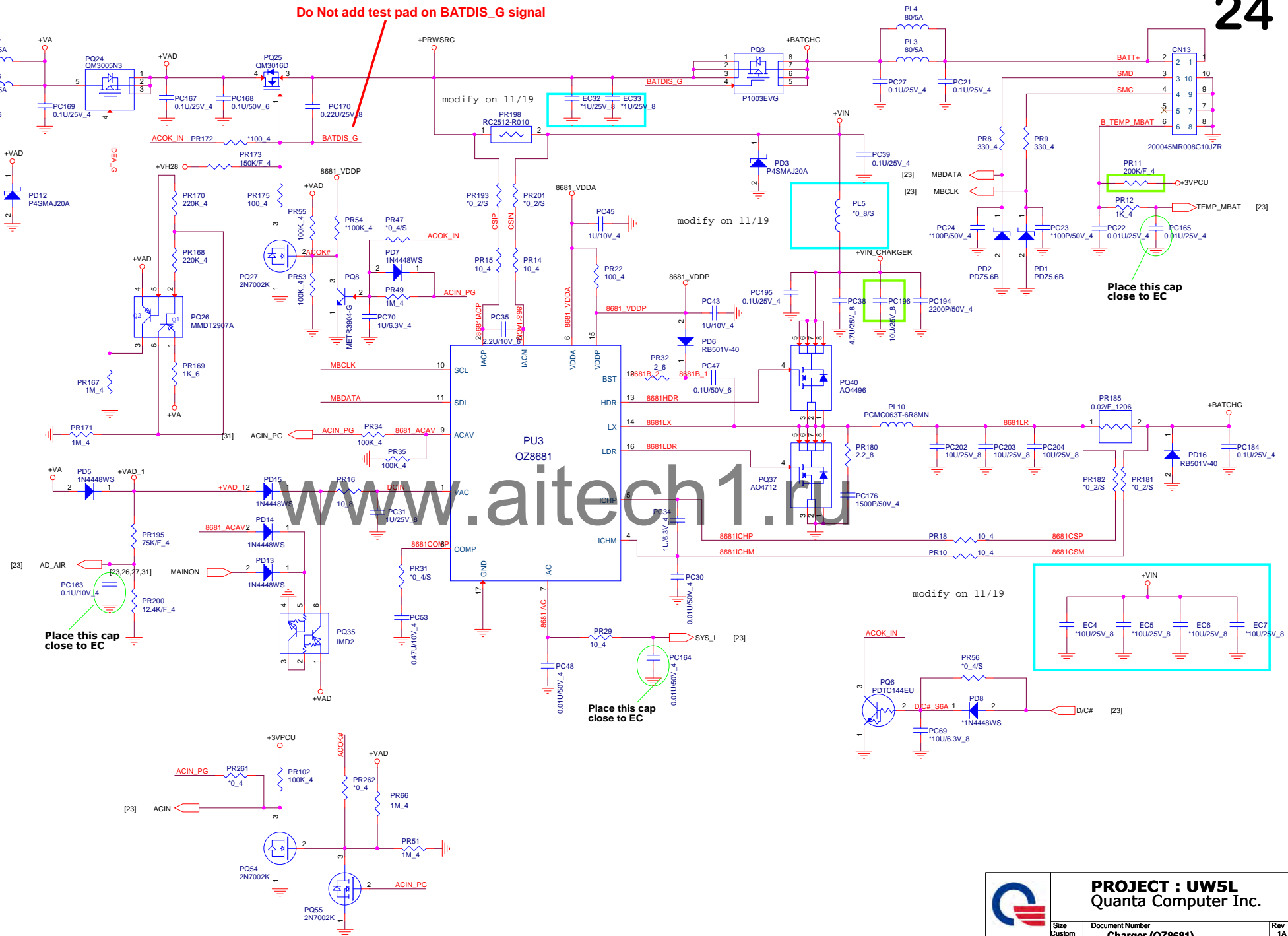


Close to U21 For EMI



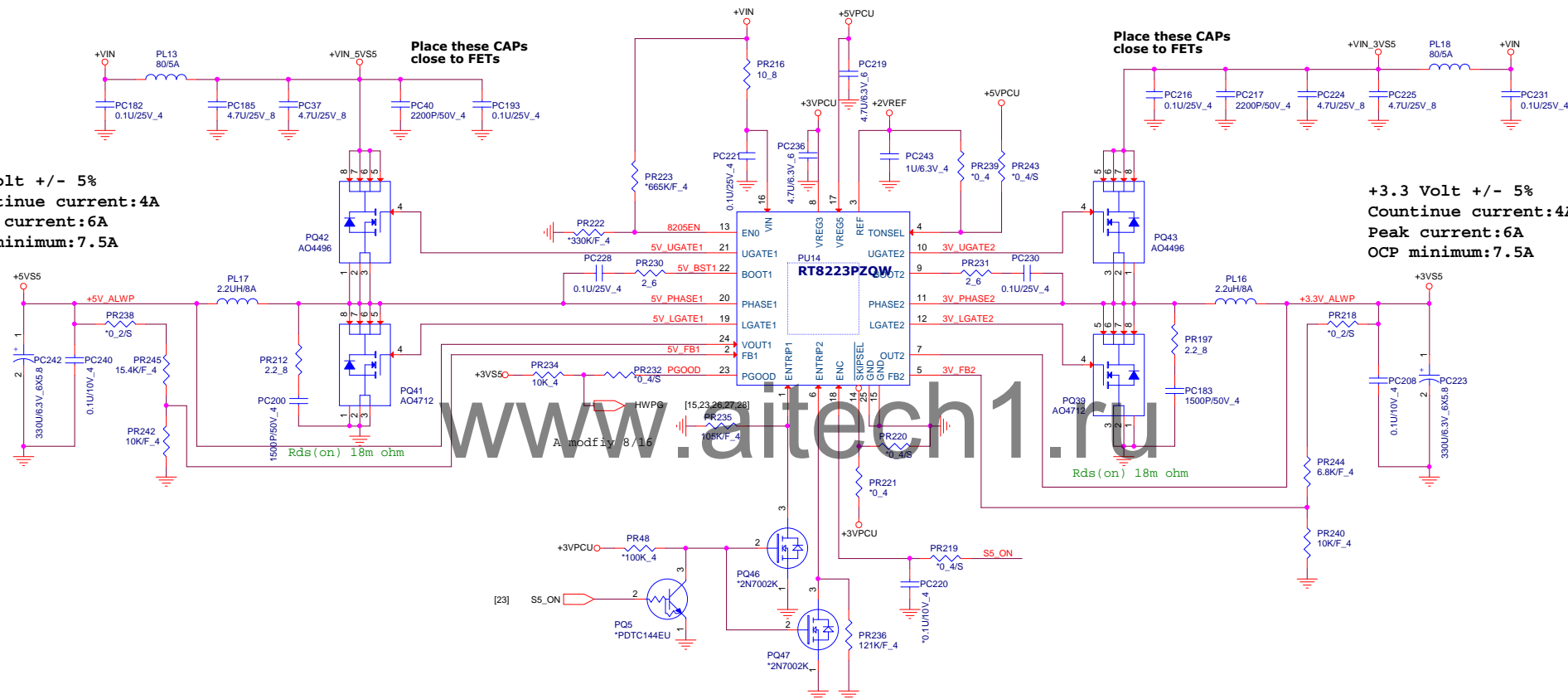


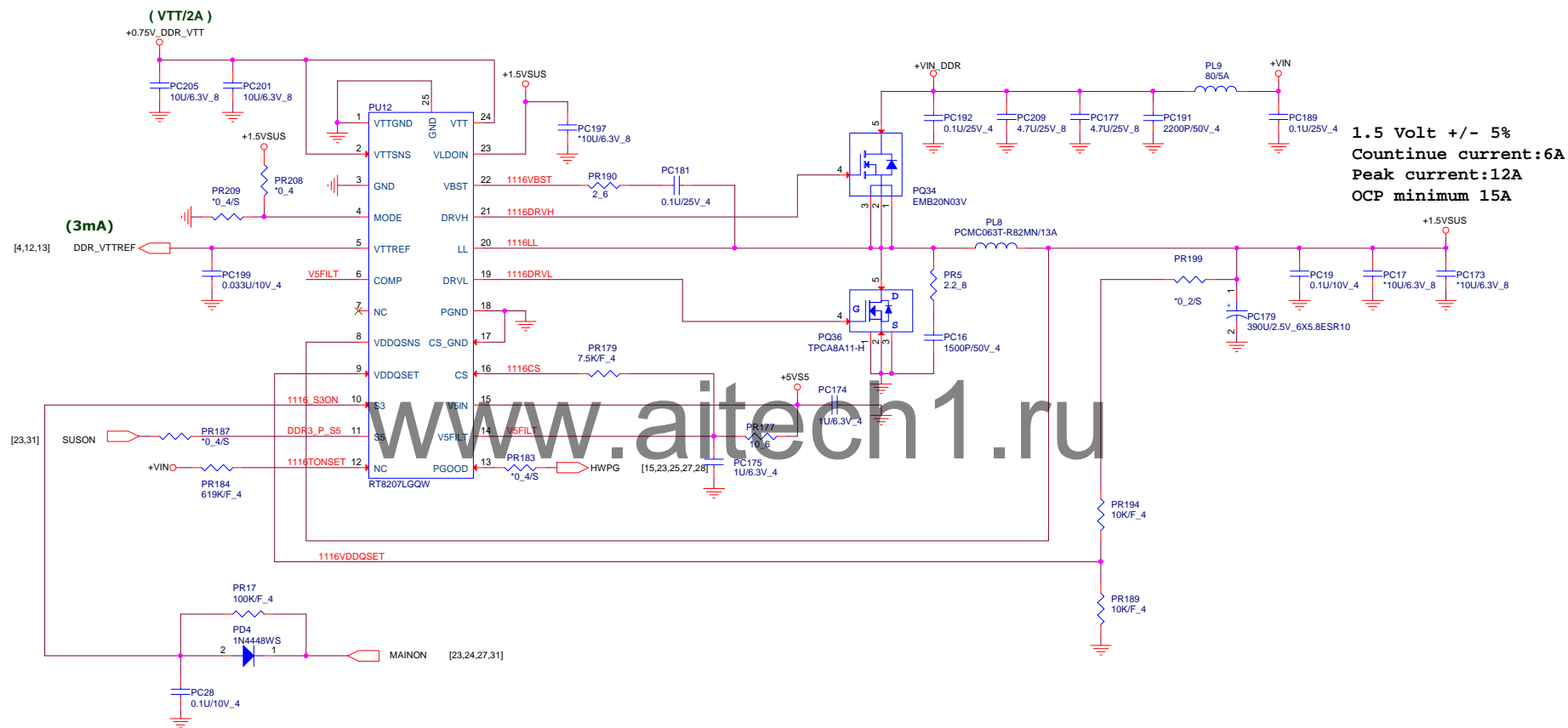
**TOP DC JACK
65W/90W**

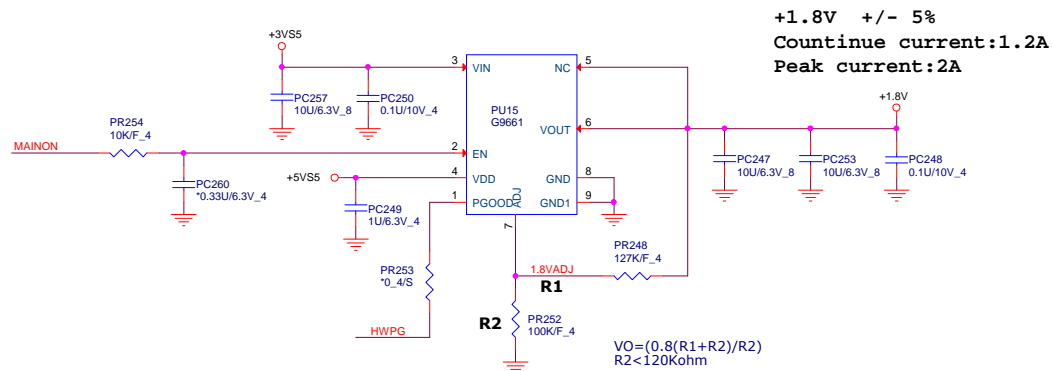
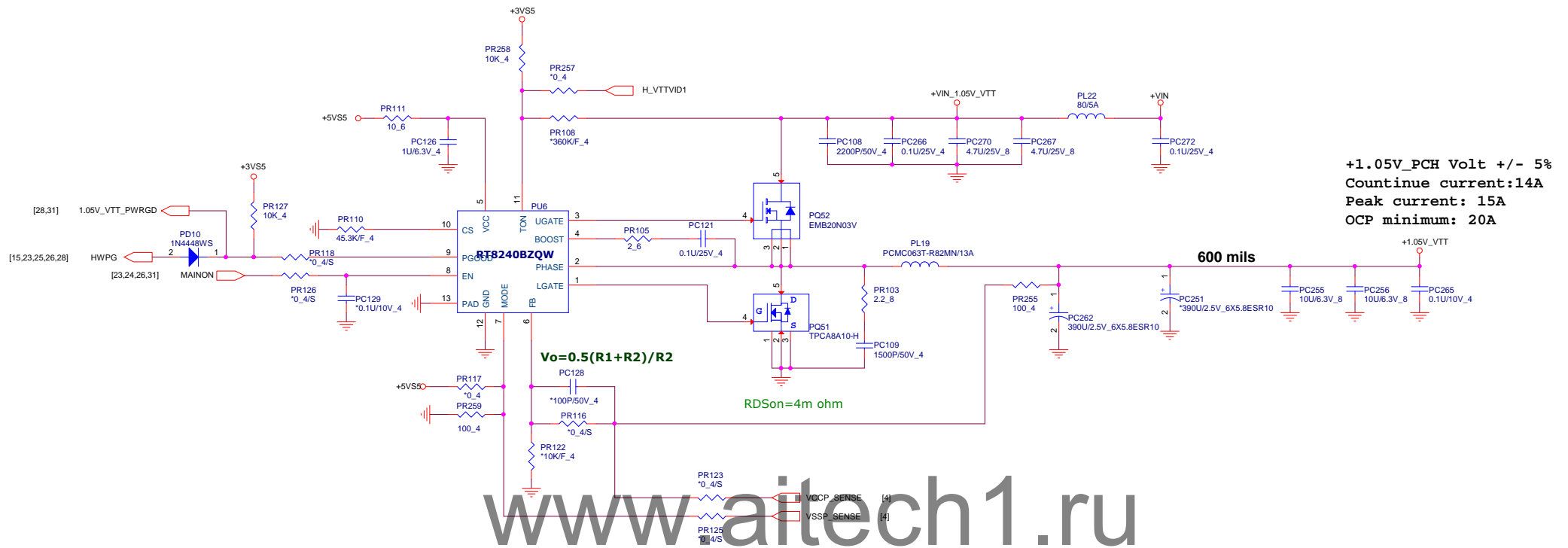


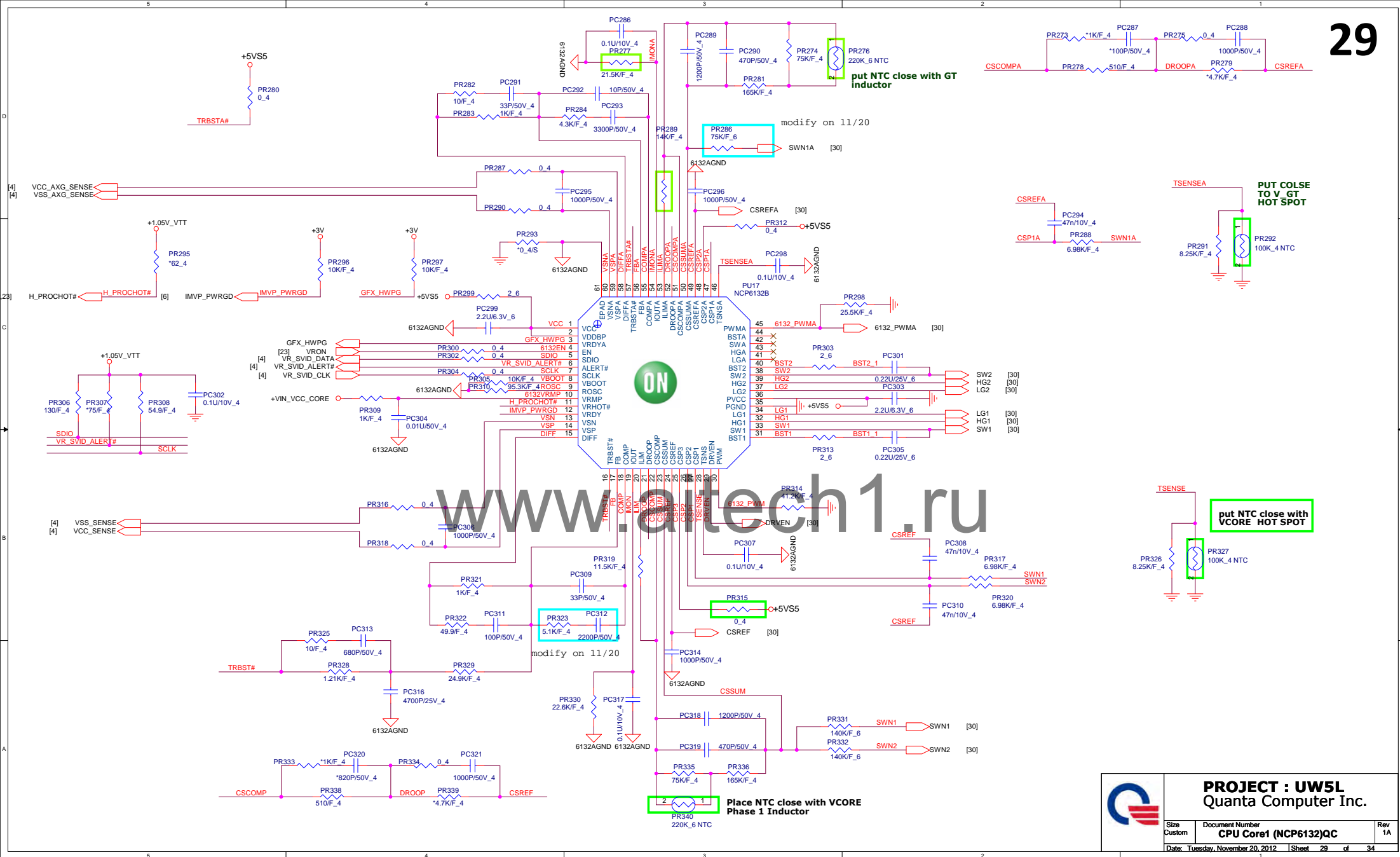
+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCp minimum:7.5A

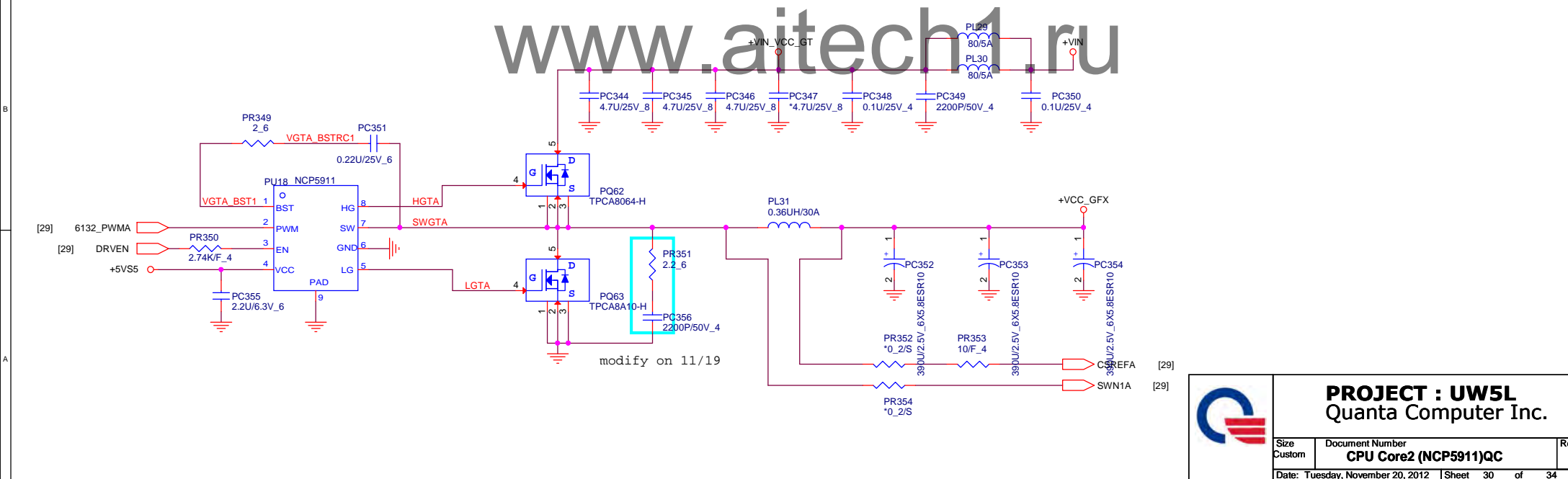
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCp minimum:7.5A



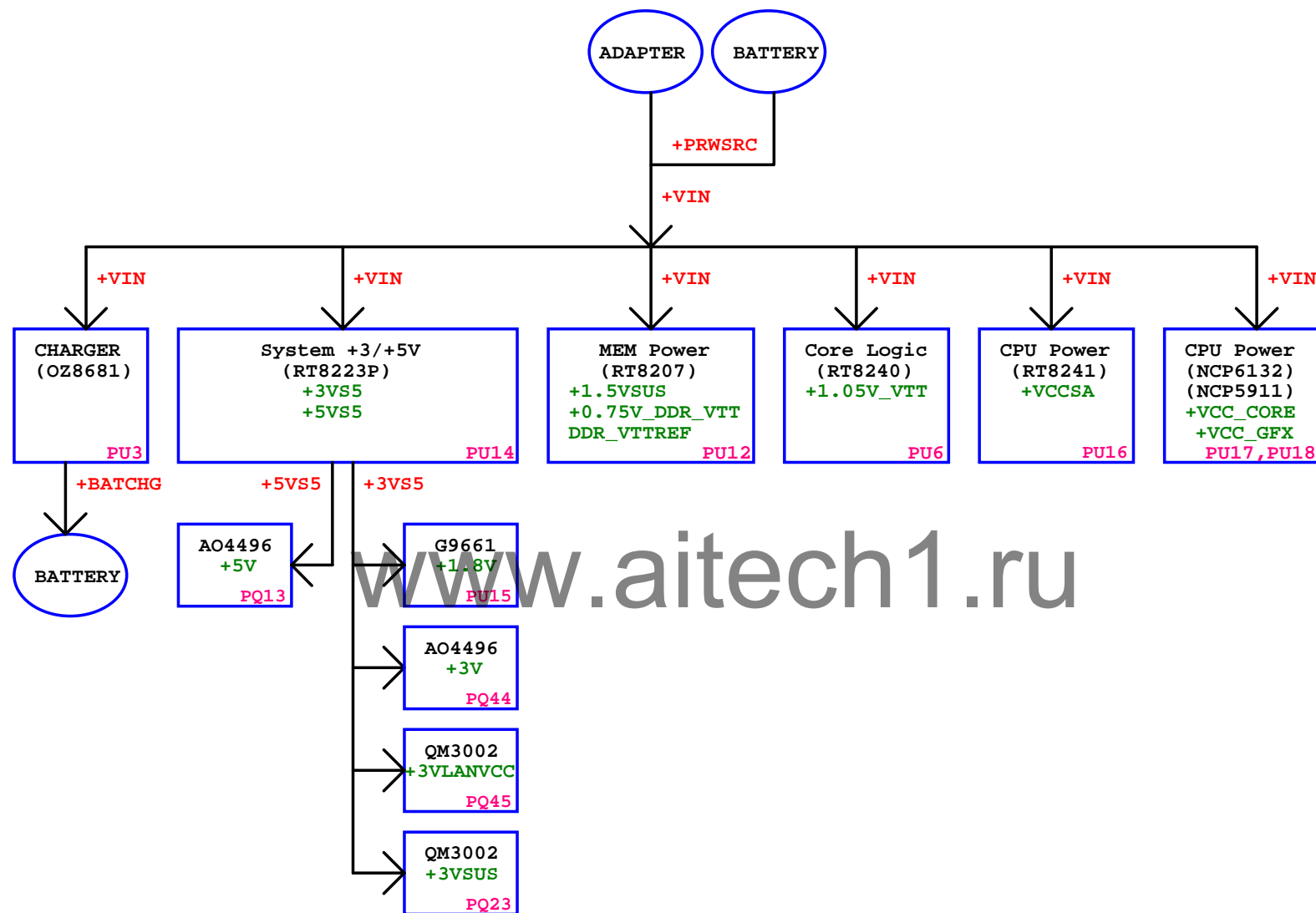






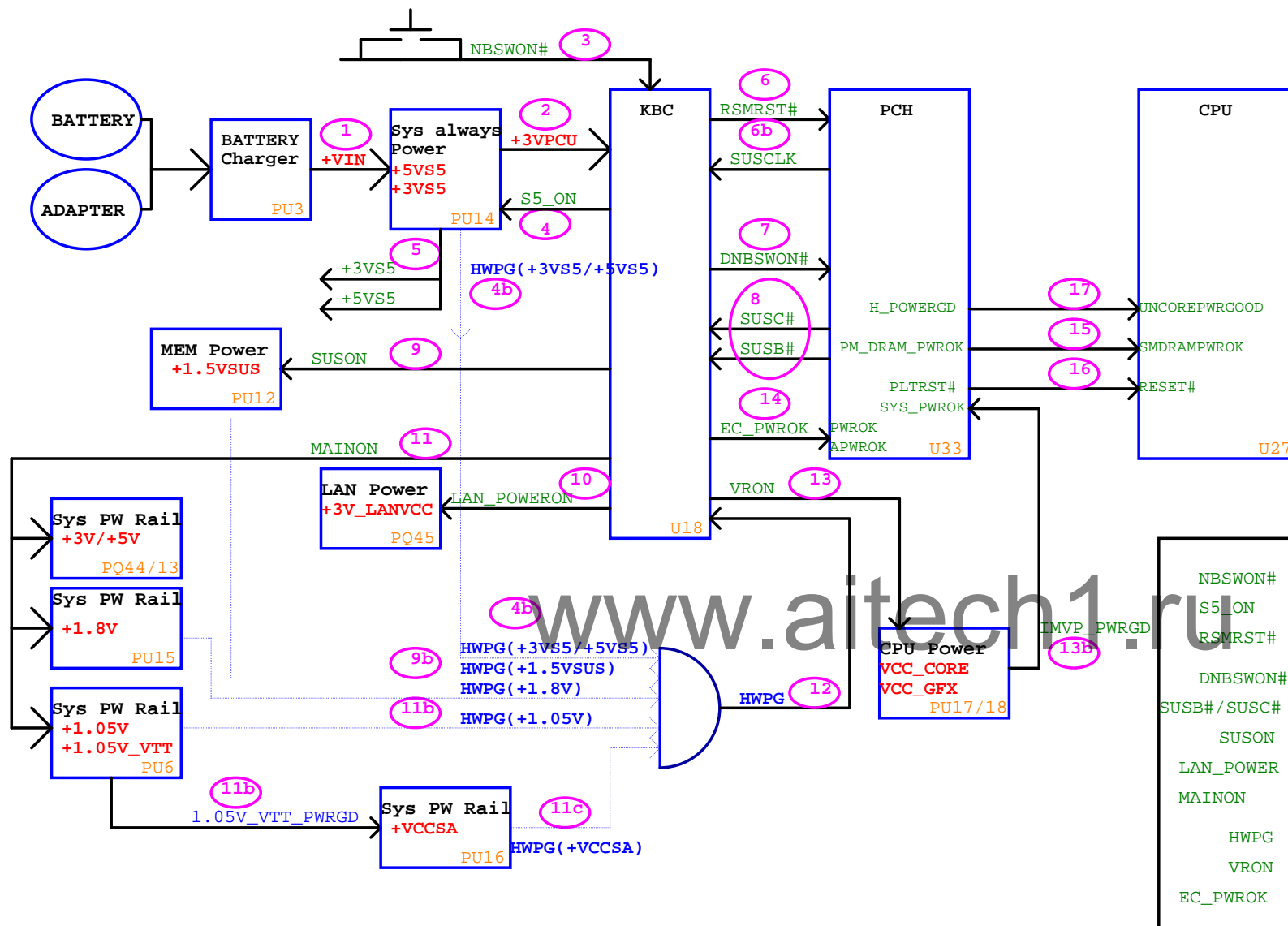


Main Power Tree



Chief River mainly Power On Sequence(G3 to S0)





EC simply control sequence

